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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Atsushi SHIMODA et al.

Serial No.: 09/783,604

Filed: February 15, 2001

For: **METHOD FOR ANALYZING CIRCUIT PATTERN DEFECTS
AND A SYSTEM THEREOF**

Group: 2623

Examiner: Virginia M. Kibler

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APR 07 2004

Technology Center 2600

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 2, 2004

Sir:

In response to the Office Action (Paper No. 4) dated on December 2, 2003,
please amend the above-identified application as follows.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims begin on page 10 of this paper.

Remarks/Arguments begin on page 20 of this paper.